REMARKS

This paper is in response to the final official action dated June 2, 2006. Reconsideration is requested.

The official action and references relied upon by the examiner have been carefully reviewed. Entry of the above amendments is respectfully requested. Claims 4-13 and 17-19 are currently pending. Independent claims 4 and 17 have been amended for clarity without adding new matter.

Claims 4-13

Claims 4, 5, and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofmann (US 6,716,754 B2) in view of Chen et al. (US 5,858,869).

Claims 4-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al in view of Hofmann as applied above, and further in view of Venkatraman et al. (US 2003/0141499 A1).

Both rejections rely on the Hofmann reference, and are respectfully traversed.

Amended claim 4 recites a method of forming metal wires, including the steps of c) adhering a plate in which a plurality of implantation holes are formed and a sidewall of a given height is formed at its edge, an engraved pattern for forming a plurality of trenches formed on the plate, and an engraved pattern for forming a plurality of via holes formed on the engraved pattern for forming the trench, onto a silicon substrate and d) injecting a low-dielectric insulating material of a liquid state or a sol or gel state completely into a space through the implantation holes and then annealing the low-dielectric insulating material.

Hofmann does not teach or suggest step d) i.e., injecting a low-dielectric insulating material of a liquid state or a sol or gel state completely into a space through implantation holes.

Referring to Fig. 8 of Hofmann, a mass 28 is formed, and a mold 300 is thus pressed downwardly into the mass 28. As a result, the mass 28 is pressed upwardly into a pattern within the openings 310, 312, 314 on the underside of the mold 300.

However, as illustrated in Figs. 3B and 3C, in the present application, a plate 20 is adhered onto a silicon substrate before forming a low-dielectric insulating material 307 and then, the low-dielectric insulating material 307 in a liquid state or a sol or gel state is injected downwardly into a space of the plate 20 from up to down through implantation holes 20c. Thus, according to the invention, the dielectric insulating material of the invention is formed in an entirely different way than in Hofmann, resulting in reductions in defects that adversely affect yield and reliability of the resulting device.

None of Chen, Zhao, and Venkatraman teach or suggest injecting a low-dielectric insulating material of a liquid state or a sol or gel state completely into a space through implantation holes.

Accordingly, amended claim 4 is clearly different from what is disclosed in Hofmann and the other applied references. It is submitted that dependent claims 5-13 are also in condition for allowance.

Claims 17-20

Claims 17-20 have also been rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al., in view of Hofmann and Venkatraman et al. Reconsideration is requested.

Amended claim 17 also recites a method of forming metal wires, including the steps of c) adhering a plate in which a plurality of first and second implantation holes are each formed and a sidewall of a given height is formed at its edge, an engraved pattern for forming a plurality of trenches formed on the plate, and an engraved pattern for forming a plurality of via holes formed on the engraved pattern for forming the trench, onto a silicon substrate, d)

injecting a first insulating material of a liquid state or a sol or gel state of a given amount through the first implantation hole and then forming a first annealing process, e) injecting a second insulating material of a liquid state or a sol or gel state through the second implantation hole and then forming a second annealing process and f) removing the plate to obtain an insulating film pattern of a multi-layer structure having the plurality of the trenches shaped by the engraved pattern for forming the trenches and the plurality of the via holes shaped by the engraved pattern for forming the via holes.

Hofmann does not teach steps d) and e).

The pattern of dielectric layer in Hofmann is formed by compression of a mold.

Referring to Figs. 5B-5F of the present application, a first or second insulating material 507a, 507b is formed by injecting the first or second insulating material in a liquid state or a sol or gel state through first or second implantation holes 40c, 40d forming up the plate 40 from the silicon substrate.

Also, in the present invention, the plate 40 is used once to form the first and second insulating material. That is, only a single process is performed to form the first and second insulating material. In contrast, the mold of Hofmann is used twice to form the first dielectric layer and the barrier layer. That is, two processes are performed, or two different molds are used in Hofmann. It is clear that the process of Hofmann would be more complicated than the method of the present claims.

Zhao and Venkatraman do not teach or suggest the steps d) and e).

Accordingly, it is believed that claims 17-20 are is clearly different form what is disclosed in Hofmann and/or Zhao and/or Venkatraman.

Therefore, the examiner is respectfully requested to pass this application to issue.

Should the examiner wish to discuss the foregoing or any matter of form in an effort to advance this application toward allowance, she is urged to telephone the undersigned at the indicated number.

Respectfully submitted,

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